

What is claimed is:

1. An arbitration parameter generating circuit comprising:

a counter which receives a request signal generated in order for a master block to occupy a system bus and a grant signal generated in order for an arbitrator to allow the master block to occupy the system bus, up-counts when the request signal is at a first logic level, down-counts when the grant signal is at the first logic level, and is reset in response to a predetermined short term reference time signal;

a short term arbitration parameter storage unit which receives and stores the counted signal as the short term arbitration parameter until the counter is reset in response to the short term reference time signal;

a short term reference time measurement unit which generates the short term reference time signal in response to the clock signal whenever the short term reference time is over, in which the short term reference time indicates a time period for which the short term arbitration parameter is stored in the short term arbitration parameter storage unit;

a long term arbitration parameter control unit which continuously accumulates the short term arbitration parameter outputted from the short term arbitration parameter storage unit, outputs the accumulated short term arbitration parameter as a long term arbitration parameter, and is reset in response to the long term reference time signal; and

a long term reference time measurement unit which generates the long term reference time signal in response to the short term reference time signal whenever the long term reference time is over.

2. The arbitration parameter generating circuit of claim 1, wherein the long term arbitration parameter control unit comprises:

an adder which continuously accumulates the short term arbitration parameter outputted from the short term arbitration parameter storage unit;

a register which stores output of the adder and is reset in response to the long term reference time signal; and

a long term arbitration storage unit which stores output of the register as the long term arbitration parameter in response to the long term reference time signal.

3. The arbitration parameter generating circuit of claim 2, wherein the long term reference time measurement unit comprises:

a long term counter which counts the number of generations of the short term reference time signal and is reset in response to the long term reference time signal; and

a long term comparing unit which previously stores the time when the long term arbitration parameter is stored in the long term arbitration parameter storage unit as the long term reference time, and generates the long term reference time signal when output of the long term counter reaches the long term reference time.

4. The arbitration parameter generating circuit of claim 2, wherein the long term reference time signal is generated at or before every 2^{n-p} times of the time when the short term reference time signal is generated, in which n denotes a bit width of the adder, and p denotes the number of bits of the short term arbitration parameter outputted from the short term arbitration parameter storage unit.

5. The arbitration parameter generating circuit of claim 1, wherein the short term reference time measurement unit comprises:

a short term counter which counts the clock signal and is reset in response to the short term reference time signal; and

a short term comparing unit which previously stores the time when the short term arbitration parameter is stored in the short term arbitration parameter storage unit as a short term reference time and generates the short term reference time signal when output of the short term counter reaches the short term reference time.

6. The arbitration parameter generating circuit of claim 5, wherein the short term reference time signal is generated at or before every 2^m times of a period of the clock signal, in which m denotes a bit width of the short term counter.

7. The arbitration parameter generating circuit of claim 1, wherein the short term arbitration parameter is calculated by subtracting the number of generations of the grant signal at the first logic level from the number of generation of the request signal at the first logic level.

8. The arbitration parameter generating circuit of claim 1, wherein the short term arbitration parameter is only the upper p bits selected from output of the counter.

9. A bus using parameter generating circuit comprising:
a counter which up-counts data in response to a clock signal, while the data is transferred via a system bus, and is reset in response to a predetermined short term reference time signal;

a short term bus using parameter storage unit which receives and stores up-counted data as a short term bus using parameter until the counter is reset in response to the short term reference time signal;

a short term reference time measurement unit which generates the short term reference time signal whenever the short term reference time is over, the short term reference time indicating a time period for which the short term bus using parameter is stored in the short term bus using parameter storage unit;

a long term bus using parameter control unit which continuously accumulates the short term bus using parameter outputted from the short term bus using parameter storage unit for a predetermined time, outputs the accumulated short term bus using parameter as a long term bus using parameter and is reset in response to a predetermined long term reference time signal; and

a long term reference time measurement unit which generates the long term reference time signal in response to the short term reference time signal whenever the long term reference time is over.

10. The bus using parameter generating circuit of claim 9, wherein the long term bus using parameter control unit comprises:

an adder which continuously accumulates the short term bus using parameter outputted from the short term bus using parameter storage unit;

a register which stores output of the adder and is reset in response to the long term reference time signal; and

5 a long term bus using parameter storage unit which stores output of the register as the long term bus using parameter in response to the long term reference time signal.

11. The bus using parameter generating circuit of claim 10, wherein the long
10 term reference time measurement unit comprises:

a long term counter which counts the number of generations of the short term reference time signal and is reset in response to the long term reference time signal; and

15 a long term comparing unit which previously stores the time when the long term arbitration parameter is stored in the long term arbitration parameter storage unit as the long term reference time, and generates the long term reference time signal when output of the long term counter reaches the long term reference time.

12. The bus using parameter generating circuit of claim 10, wherein the long
20 term reference time signal is generated at or before every 2^{n-p} times of the time when the short term reference time signal is generated, in which n denotes a bit width of the adder, and p denotes the number of bits of the short term bus using parameter outputted from the short term bus using parameter storage unit.

13. The bus using parameter generating circuit of claim 9, wherein the short
25 term reference time measurement unit comprises:

a short term counter which counts the clock signal and is reset in response to the short term reference time signal; and

30 a short term comparing unit which previously stores the time when the short term arbitration parameter is stored in the short term arbitration parameter storage unit as a

short term reference time and generates the short term reference time signal when output of the short term counter reaches the short term reference time.

14. The bus using parameter generating circuit of claim 13, wherein the short term reference time signal is generated at or before every 2^m times of a period of the clock signal, in which m denotes a bit width of the short term counter.

15. The bus using parameter generating circuit of claim 9, wherein the short term bus using parameter is equal to the number of data transfers via the system bus.

16. The bus using parameter generating circuit of claim 9, wherein the short term bus using parameter is only the upper p bits selected from output of the counter.

17. A system on chip including a system bus, first through n^{th} master blocks that transfer data via the system bus, and an arbitrator that controls occupation of the system bus by the master blocks, the system on chip comprising:

a bus using parameter control circuit which measures the number of data transfers via the system bus for a predetermined short term reference time in response to a predetermined short term reference time signal, generates the measured number as a short term bus using parameter, and generates a short term bus using parameter, which is accumulated during a predetermined time, as a long term bus using parameter in response to a predetermined long term bus using parameter signal;

a short term reference time measurement unit which generates the short term reference time signal in response to a clock signal whenever the short term reference time is over; and

a long term reference time measurement unit which generates the long term reference time signal in response to the short term reference time signal whenever a predetermined long term reference time is over,

wherein each of the first through n^{th} master blocks includes an arbitration parameter control circuit which receives a request signal generated for the master blocks to occupy the system bus and a grant signal generated for the arbitrator to allow

the master blocks to occupy the system bus, counts the number of generations of the request signals and the grant signals at a first logic level in response to the short term reference time signal, generates a short term arbitration parameter, continuously accumulates the short term arbitration parameter for a predetermined time in response to the long term reference time signal and generates the accumulated short term arbitration parameter as a long term arbitration parameter.

18. The system on chip of claim 17, wherein the bus using parameter control circuit comprises:

a bus counter which up-counts the data in response to the clock signal, while the data are transferred via the system bus, and is reset in response to the short term reference time signal;

a short term bus using parameter storage unit which receives and stores the up-counted data as the short term bus using parameter in response to the short term reference time signal until the bus counter is reset; and

a long term bus using parameter control unit which continuously accumulates the short term bus using parameter outputted from the short term bus using parameter storage unit during a predetermined time, outputs the accumulated short term bus using parameter as the long term bus using parameter, and is reset in response to a predetermined long term reference time signal.

19. The system on chip of claim 18, wherein the long term bus using parameter control unit comprises:

a bus adder which continuously accumulates the short term bus using parameter outputted from the short term bus using parameter storage unit;

a bus register which stores output of the adder and is reset in response to the long term reference time signal; and

a long term bus using parameter storage unit which stores output of the register as the long term bus using parameter in response to the long term reference time signal.

20. The system on chip of claim 17, wherein the arbitration parameter control circuit comprises:

a counter which receives the request signal and the grant signal, up-counts when the request signal is at a first logic level, and down-counts when the grant signal is at the first logic level, and is reset in response to a predetermined short-time reference time signal;

a short term arbitration parameter storage unit which receives and stores the counted signals as a short term arbitration parameter in response to the short term reference time signal until the counter is reset; and

a long term arbitration parameter control unit which continuously accumulates the short term arbitration parameter outputted from the short term arbitration parameter storage unit, outputs the accumulated short term arbitration parameter as a long term arbitration parameter and is reset in response to a predetermined long term reference time signal.

21. The system on chip of claim 17, wherein the long term arbitration parameter control unit comprises:

an adder which continuously accumulates the short term arbitration parameter outputted from the short term arbitration parameter;

a register which stores output of the adder and is reset in response to the long term reference time signal; and

a long term arbitration storage unit which stores output of the register as the long term arbitration parameter in response to the long term reference time signal.

22. A method of generating an arbitration parameter which decides priority of master blocks transferring data via a system bus, the method comprising:

(a) generating a short term reference time signal which decides the time when storing a predetermined short term arbitration parameter in response to a clock signal;

(b) receiving a request signal generated for the master blocks to occupy the system bus and a grant signal generated for the arbitrator to allow the master blocks to

occupy the system bus and generating a short term arbitration parameter in response to the short term reference time signal;

(c) generating a long term reference time signal which decides the time when storing a predetermined long term arbitration parameter in response to the short term reference time signal; and

(d) continuously accumulating the short term arbitration parameter for a predetermined time in response to the long term reference time signal and outputting the accumulated short term arbitration parameter as a long term arbitration parameter.

23. The method of claim 22, wherein step (b) further comprises:

(b1) up-counting when the request signal is at the first logic level, down-counting when the grant signal is at the first logic level and outputting the counted value as a short term arbitration parameter; and

(b2) resetting the counted signal in response to the short term reference time signal and counting the request signal and the grant signal according their logic level.

24. The method of claim 22, wherein the short term arbitration parameter is calculated by subtracting the number of generations of the grant signal at the first logic level from the number of generations of the request signal at the first logic level.

25. The method of claim 22, wherein step (d) further comprises:

(d1) continuously accumulating the short term arbitration parameter and outputting the accumulated short term arbitration parameter as the long term arbitration parameter; and

(d2) resetting the accumulated short term arbitration parameter in response to the long term reference time signal, continuously accumulating the short term arbitration parameter and outputting the accumulated short term arbitration parameter as the long term arbitration parameter.

26. The method of claim 22, wherein the short term reference time signal is generated at a shorter interval than the long term reference time signal.

27. A method of generating a bus using parameter which decides priority of master blocks transferring data via a system bus, the method comprising:

(a) generating a short term reference time signal which decides a time to store a predetermined short term bus using parameter in response to a clock signal;

(b) up-counting data in response to the clock signal and the short term reference time signal whenever the data are transferred via the system bus and outputting the counted data as the short term bus using parameter;

(c) generating a long term reference time signal which decides a time to accumulate the short term bus using parameter in response to the short term reference time signal; and

(d) continuously accumulating the short term bus using parameter for a predetermined time in response to the long term reference time signal and outputting the accumulated short term bus using parameter as a long term bus using parameter.

28. The method of claim 27, wherein step (b) further comprises:

(b1) up-counting data in response to the clock signal while the data are transferred via the system bus and outputting the counted data as the short term bus using parameter; and

(b2) resetting the counted data in response to the short term reference time signal, and up-counting reset data in response to the clock signal while the data are transferred via the system bus and outputting the counted data as the short term bus using parameter.

29. The method of claim 24, wherein the short term bus using parameter is the number of data transfers via the system bus.

30. The method of claim 27, wherein step (d) further comprises:

(d1) continuously accumulating the short term bus using parameter and outputting the accumulated short term bus using parameter as a long term bus using parameter; and

(d2) resetting the accumulated short term bus using parameter in response to the long term reference time signal, and continuously accumulating the reset short term bus using parameter and outputting the accumulated short term bus using parameter as a long term bus using parameter.

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31. The method of claim 27, wherein the short term reference time signal is generated at a shorter interval than the long term reference time signal.